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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/008,525	06/29/1998	YOUNG-WOO PARK	2557-000048/US	6330

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/008,525	YOUNG-WOO PARK ET AL	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) *4,7-15,19-43 and 47-55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,16-18 and 44-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-2, 16-18 and 44-46, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (fig. 1, pages 1-2) in view of Chang et al. [U.S. Pat. 6,025,247] previously applied.

With respect to claims 1-2 and 44-46, Applicant Admitted Prior Art discloses a method for manufacturing a semiconductor memory device comprising the steps of:

forming a pad (14) on a semiconductor substrate (100);

forming a first insulating layer (16) on a semiconductor substrate (100);

forming a plurality of bit lines (18,20) on the first insulating layer, each of the plurality of bit lines including at least one bit line layer (18 or 20);

forming a second insulating layer (22) on the plurality of bit lines;

forming a contact hole exposing the pad (14) on the semiconductor substrate by patterning the second insulating layer, and the first insulating layer;

forming a storage electrode (30) over the second insulating layer and connected to the portion of the semiconductor substrate through the contact hole; and

sequentially forming a dielectric layer (32) and a plate electrode (34) on the storage electrode.

Applicant Admitted Prior Art fails to disclose forming an oxidation preventing layer (nitride layer) over substantially the entire surface of the bit lines and the first insulating layer; the oxidation preventing layer remaining interposed between the contact hole and the bit lines; and the oxidation preventing layer arranged to contact all of the at least one bit line layers.

However, Chang et al. discloses forming an oxidation preventing layer (315) (nitride layer) over substantially the entire surface of the bit lines (313) and the first insulating layer (303) (fig. 3g, col. 7, lines 40-41); the oxidation preventing layer (315) remaining interposed between the contact hole (318, 319) and the bit lines (313); and the oxidation preventing layer arranged to contact all of the at least one bit line layers (fig. 3h). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to form the oxidation preventing layer (nitride layer) over the entire surface of the bit lines and the first insulating layer; the oxidation preventing layer

remaining interposed between the contact hole and the bit lines; and the oxidation preventing layer arranged to contact all of the at least one bit line layers as taught by Chang et al. into the process of Applicant Admitted Prior Art in order to use as an etching stop layer for protecting the bit lines (col. 7, lines 42-43).

With respect to claim 16, Applicant Admitted Prior Art discloses that the contact hole has a sidewall (28) and wherein the step of forming a storage electrode is preceded by a step of forming a spacer on the sidewall of the contact hole.

With respect to claim 17, Applicant Admitted Prior Art discloses that the first and second insulating layers comprise a borophosphosilicate glass (BPSG) or an undoped silicate glass (USG) (pages 1-2).

With respect to claim 18, Applicant Admitted Prior Art discloses that a nitride layer (24) and an oxide layer (26) are sequentially formed on the second insulating layer prior to the step of forming the contact hole.

4. Claims 3 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art in view of Chang et al. [U.S. Pat. 6,025,247] previously applied, as applied to claims 1-2 above, and further in view of Lu et al. IU.S. Pat. 5,595,928] previously applied.

The combination of Applicant Admitted Prior Art and Chang et al. disclose all the limitation as claimed above except the nitride layer is formed by LPCVD at temperature of about 800-1000° C under a pressure of about 1 torr or less using a gas mixture of dichlorosilane and ammonia as a reactant gas and a thickness equal to or less than about 1,000 angstroms. However, Lu et al. discloses that using a gas mixture of dichlorosilane and ammonia as a reactant gas at temperature of about 700-800° C to form the nitride layer (26) with the thickness equal to or less than about 1,000 angstroms (col. 5, lines 37-46). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to use a gas mixture of dichlorosilane and ammonia as a reactant gas as taught by Lu et al. into the process of Chang et al. in order to form a conformal nitride layer (see col. 5, lines 37-38).

It is noted that, the temperature, thickness and pressure range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

5. Applicant's arguments filed May 15, 2006 have been fully considered but they are not persuasive.

Applicant argues that Chang fails to disclose that the silicon nitride layer 315 contacts the silicide layer 309 of the bit line structure 313.

Applicant's argument is not persuasive because the claim does not require the silicon nitride layer to contact the silicide layer.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

8. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-872-9306.

HOAI PHAM
PRIMARY EXAMINER